In the Specification:

Please replace the paragraph beginning on page 1, line 13, with the following written paragraph:

A liquid crystal display panel is as small as a few inches and has relatively small delay of time due to the resistances of interconnection lines.

Please replace the paragraph beginning on page 3, line 18, with the following written paragraph:

However, when the panel 16 has a large size of 10 inches or more, each line of the 24-bit data buses 22 has a resistance of 10 kΩ or more. Additionally, the resistance of the display signal lines 30 cannot be neglected. The resistance of the display signal lines 30 can be reduced if an increased number of lines 30 is used, as shown in Fig. 3. The structure shown in Fig. 3 employs 300 display signal lines to which display signals D1-D300 are respectively applied. The display signal lines 42 can be driven by a general – purpose data driver IC marketed. When a increased number of display signal lines is used, the display data can be written onto the data buses 22 for a longer time. Hence, the width of each of the display signal lines 42 can be reduced. However, the total width of the display signal lines 42 is approximately equal to 6.0 mm. This increases the size of the peripheral circuits with regard to the panel 16.

Please replace the paragraph beginning on page 4, line 31, with the following written paragraph:

The above object of the present invention is achieved by a liquid crystal display device comprising: a liquid crystal display panel; a data driver connected to the liquid crystal display panel; and a gate driver connected to the liquid crystal display panel. The data driver is divided into a plurality of blocks, which simultaneously supply the liquid crystal display panel with display signals respectively supplied thereto. Hence, each of the blocks has a reduced number of display signal lines, which reduces an area for arranging the display signal lines. Hence, the cross-coupling capacitance can be reduced.

Please replace the paragraph beginning on page 9, line 18, with the following written paragraph:

Eight-bit signals 86A, 86B and 86C are applied to the respective eight-bit digital latch circuits of the same group from the display signal supply device 114. The signal 86A consists of eight bits of display data R. The signal 86B consists of eight bits of display data B. The signal 86C consists of eight bits of display data C. The three latch circuits 88 of the same group are supplied with the shift pulse from the shift register 80 and simultaneously latch the eight-bit signals 86A-86C, respectively. Then, the next three latch circuits 88 of the same group are supplied with the shift pulse from the shift register 80 and simultaneously the

eight-bit signals 86A-86C, respectively. In the above manner, the digital eight-bit latch circuits 88 are sequentially selected. When all the 300 latch circuits 88 have latched the corresponding eight-bit digital signals, a latched enable signal LE is applied to the digital eight-bit latch circuits 92, which simultaneously latch the eight-bit display signals from the corresponding latch circuits 88.

Please replace the paragraph beginning on page 12, line 31, with the following written paragraph:

After the select signal rd is applied, the latch enable signal LE is activated, and the 300 bits of display data latched in the circuit 88 are latched in the digital eight-bit latch circuits 92 shown in Fig. 8. When the latch enable signal LE is high and active, all the output select signals ra-rd are low and are thus inactive. This is intended to satisfy that the general driver IC device 76 is required to inhibit the device 76 from latching next data for a given time equal to, for example, 5 clocks while the previous data is output.

Please replace the paragraph beginning on page 18, line 37, with the following written paragraph:

Fig. 19 is a circuit diagram of each of the D/A converters 94, which converts the eight-bit digital signal into a corresponding analog signal. The D/A converter 94 includes transistors 140-147 which implement resistors of different resistance values, and gate